FORM PTO-1390 (REV 5-93) US DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. §371

ATTORNEY DOCKET NUMBER: 2001-0244A

U.S. APPLICATION NO. (If known, see 37 CFR 1.5): NEW 09778482

International Application No.	International Filing Date	Priority Date Claimed
PCT/JP00/04475	July 5, 2000	July 6, 1999

Title of Invention
DIGITAL SIGNAL PROCESSOR

Applicant(s) For DO/EO/US
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Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. [X] This is a **FIRST** submission of items concerning a filing under 35 U.S.C. §371.

2. [] This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. §371.

3. [X] This express request to begin national examination procedures (35 U.S.C. §371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. §371(b) and PCT Articles 22 and 39(1).

4. [] A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.

5. [X] A copy of the International Application as filed (35 U.S.C. §371(c)(2))
   a. [] is transmitted herewith (required only if not transmitted by the International Bureau).
   b. [X] has been transmitted by the International Bureau. **ATTACHMENT A**
   c. [] is not required, as the application was filed in the United States Receiving Office (RO/US)

6. [X] A translation of the International Application into English (35 U.S.C. §371(c)(2)). **ATTACHMENT B**

7. [] Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. §371(c)(3)).
   a. [] are transmitted herewith (required only if not transmitted by the International Bureau).
   b. [] have been transmitted by the International Bureau.
   c. [] have not been made; however, the time limit for making such amendments has NOT expired.
   d. [] have not been made and will not be made.

8. [] A translation of the amendments to the claims under PCT Article 19.

9. [X] An oath or declaration (unexecuted) of the inventor(s) (35 U.S.C. §371(c)(4)). **ATTACHMENT C**

10. [] A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. §371(c)(5)).

Items 11. to 14. below concern other document(s) or information included:

11. [X] An Information Disclosure Statement under 37 CFR 1.97 and 1.98. **ATTACHMENT D**

12. [] An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.

13. [] A FIRST preliminary amendment.

    [] A SECOND or SUBSEQUENT preliminary amendment.

14. [X] Other items or information: Notification Concerning Submission or Transmittal of Priority Document -

ATTACHMENT E

U.S. APPLICATION NO. (if known) NEW 09/786482	INTERNATIONAL APPLICATION NO. PCT/JP00/04475	ATTORNEY'S DOCKET NO. 2001-0244A

15. [X] The following fees are submitted

	CALCULATIONS	PTO USE ONLY
BASIC NATIONAL FEE (37 CFR 1.492(a)(1)-(5)):		
Neither international preliminary examination fee nor international search fee paid to USPTO and International Search Report not prepared by the EPO or JPO $1000.00		
International Search Report has been prepared by the EPO or JPO ..... $ 860.00		
International preliminary examination fee not paid ot USPTO but international search paid to USPTO ..... $ 710.00		
International preliminary examination fee paid to USPTO but claims did not satisfy provisions of PCT Article 33(1)-(4) ..... $ 690.00		
International preliminary examination fee paid ot USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) ..... $ 100.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$860.00	
Surcharge of $130.00 for furnishing the oath or declaration later than [] 20 [] 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$	

Claims	Number Filed	Number Extra	Rate		
Total Claims	3 -20 =		X $18.00	$	
Independent Claims	1 - 3 =		X $80.00	$	
Multiple dependent claim(s) (if applicable)			+ $270.00	$	

TOTAL OF ABOVE CALCULATIONS =	$860.00	
[] Small Entity Status is hereby asserted. Above fees are reduced by 1/2.	$	
SUBTOTAL =	$860.00	
Processing fee of $130.00 for furnishing the English translation later than [] 20 [] 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +	$	
TOTAL NATIONAL FEE =	$860.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). $40 per property +	$	
TOTAL FEES ENCLOSED =	$860.00	
	Amount to be refunded	$
	Amount to be charged	$

a. [X] A check in the amount of $860.00 to cover the above fees is enclosed. A duplicate copy of this form is enclosed.

b. [] Please charge my Deposit Account No. 23-0975 in the amount of $_____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. [X] The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 23-0975.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

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THE COMMISSIONER IS AUTHORIZED TO CHARGE ANY DEFICIENCY IN THE FEES FOR THIS PAPER TO DEPOSIT ACCOUNT NO. 23-0975

[CHECK NO. 43332]

[2001_0244A]

DESCRIPTION

DIGITAL SIGNAL PROCESSOR

TECHNICAL FIELD

The present invention relates to a digital signal processor and, more particularly, to one that shows the effect when applied to a servo control of an optical disk apparatus.

BACKGROUND ART

Figure 9 is a diagram illustrating the construction of a servo control device in a conventional optical disk apparatus.

In this optical disk apparatus, a reflected light of a laser beam, which faced on the disk recording surface through a field lens 93 installed in an optical pickup 92 and which is emitted, is employed so as to read out data recorded in an optical disk 91. The quantity of light of the reflected light detected by employing a sensor such as a photo detector 94 is converted from analog data to digital data by an A/D converter 95 and is inputted to a digital signal processor 96. While the quantity of light of the reflected light detected varies influenced by the disk rotations, external vibrations, or the like, the quantity of light of the reflected light has to be kept at a large value so as to read out data correctly. To realize the same, it is necessary to perform a focus control and a tracking control.

The focus control is to control the field lens against the surface deflection of the disk so that a distance between the field lens 93 installed in the optical pickup and the disk recording surface should be kept in the constant and that the disk recording surface should be located within the depth of focus of the laser. The tracking control is one that controls the field lens 93 against decentering of the disk so that the optical spot should scan on the track correctly. The focus control and the tracking control are realized by detecting a focus error signal and a tracking error signal which respectively represent whether or not focusing and tracking are performed correctly from the reflected light, calculating a focus driving amount and a tracking driving amount by digital operations, and driving the field lens 93 by signals passing through D/A converters 97C and 97D, respectively. As servo controls required for the optical disk apparatus, there are a spindle control which controls a spindle motor 98 for rotating the optical disk, a traverse control for driving the optical pickup 92, and the like, other than the focus control and the tracking control.

As a construction of the digital signal processor which performs the servo control in a conventional optical disk apparatus, there is a method disclosed in Japanese Published Patent Application No. Hei. 10-255283, entitled as "A control method of an optical pickup and an optical disk apparatus". In this prior official report, there is disclosed the construction of a servo system in the optical disk device having a CPU as a main arithmetic device and a DSP as an

auxiliary arithmetic device which supplements the CPU, and a system in which various tasks required for the servo control of the optical device are processed in the CPU and the DSP divisionally.

Hereinafter, a conventional digital signal processor which comprises two arithmetic devices and performs a servo control in the optical disk apparatus will be described with reference to figure 7.

In figure 7, reference numerals 11 and 12 denote arithmetic devices, numeral 13 denotes an external bus, numerals 14 and 16 denote program memory areas, numerals 15 and 17 denote arithmetic logic units "ALU", numeral 18 denotes a task list, numeral 19 denotes an external start-up factor, numeral 70 denotes a processing pointer A, numeral 21 denotes a program counter, numeral 22 denotes an instruction decoder, numeral 23 denotes a program halt notification signal, numeral 24 denotes a termination status storage register, and numeral 25 denotes a processing demand generation circuit.

The arithmetic device 11 and the arithmetic device 12 are connected each other by the external bus 13, and it is possible that the arithmetic device 11 should refer to the internal register of the arithmetic device 12. The arithmetic device 11 makes the arithmetic logic unit 15 activated by a program stored in the program memory area 14, and calculates driving values required for the spindle control, the traverse control, or the like. Similarly, the arithmetic device 12 also makes the arithmetic logic unit 17 operated by a program stored in the program memory area 16, and calculates

driving values needed for the focus control, the tracking control, or the like.

For example, a processing A which is a focus control processing and a processing B which is a tracking control processing in the arithmetic device 12 are previously transferred from the arithmetic device 11 via the external bus 13 and are stored in the program memory area 16. Moreover, starting addresses of the processing A and the processing B are transferred from the arithmetic device 11 to the task list 18 which is established in the arithmetic device 12. The task list 18 stores the starting addresses of respective processings and execution modes of respective processings as a pair, respectively. The execution mode indicates whether the corresponding processing can be performed or not. When a high (hereinafter referred to as "Hi") pulse is inputted to the external start-up factor 19 which is generated at a constant period, the arithmetic device 12 is initialized so that the processing pointer A 70 should indicate the head of the task list 18. Further, 0 indicating no conclusion is set to the termination status storage device 24. In addition, the arithmetic device 12 copies the address stored in the task list 18 that is indicated by the processing pointer A 70 to the program counter 21. At this time, when the execution mode corresponding to the address indicated by the processing pointer A 70 indicates "0" meaning incapability of execution, the processing pointer is incremented by 1 and tries to copy the address of the following processing to the program counter 21.

According to the above-mentioned operation, the program of the processing A is activated and is read out from the program memory area 16. Then, when the program of the processing A read out is interpreted by the instruction decoder 22, the arithmetic logic unit 17 is operated to perform the processing A.

When the program counter 21 reaches the termination address of the processing A and the program halt instruction is inputted to the instruction decoder 22, the arithmetic device 12 makes the instruction decoder 22 output the program halt notification signal 23 to the processing pointer A 70. When the program halt notification signal 23 is notified to the processing pointer A 70, the arithmetic device 12 changes the indication destination to the task list 18 from the processing A to the processing B and copies the starting address of the processing B to the program counter 21. Thereby, the program of the processing B is activated to perform the processing B. The arithmetic device 12 repeats similar operations for all processings stored in the task list 18, and sets 1 indicating the conclusion of the processings to the termination status storage register 24 when all the processings are concluded.

The arithmetic device 11 monitors the termination status storage register 24 of the arithmetic device 12, and when 0 indicating that the arithmetic device 12 is not under execution of the processing is set, the arithmetic device 11 can demand the arithmetic device 12 to execute a processing C which is not stored in the task list 18, employing the processing demand generation circuit 25.

According to the so-constructed digital signal processor of the optical disk apparatus, processings can be distributed such that the focus control and the tracking control which require high operating speeds are performed by the arithmetic device 12 while the spindle control and the traverse control which only require a low working speeds are performed by the arithmetic device 11, whereby the arithmetic device 11 can be realized by an inexpensive small sized circuit.

However, according to the construction of the above-described conventional digital signal processor, when the arithmetic device 11 demands that the arithmetic device 12 should execute the processing C, the arithmetic device 11 has to monitor the termination status storage register 24, thereby resulting in a processing waiting time for the processing of the arithmetic device 12 at the arithmetic device 11. For example, as shown in a timing chart in figure 8, when the execution demand for the processing C is generated from the arithmetic device 11 while the arithmetic device 12 is performing the processing A, the arithmetic device 11 has to be in a waiting state with monitoring the termination status storage register 24 until the arithmetic device 12 concludes the processing A and the processing B.

Further, the processing C, for which the processing is demanded from the arithmetic device 11, can not be performed after the arithmetic device 12 concluded the processing A and before it starts the processing B.

In addition, it B not possible to perform the processing C, for which the processing is demanded from the arithmetic device 11, with interrupting the processing A which is under execution by the arithmetic device 12.

The present invention is made to solve the above-mentioned problems and has for its object to provide a digital signal processor which can remove the waiting time at the arithmetic device 11 as well as can change the processing order at the arithmetic device 12.

DISCLOSURE OF INVENTION

According to claim 1 of the present invention, there is provided a digital signal processor comprising: a main arithmetic device which generates a task demand; an auxiliary arithmetic device which receives the task demand from the main arithmetic device and performs the task; the auxiliary arithmetic device being provided with a reservation processing register for setting a task from the main arithmetic device even when the auxiliary arithmetic device is performing a processing; a clear circuit for clearing the task stored in the reservation processing register after the task set in the reservation processing register is performed; and the task demanded from the main arithmetic device being performed after the auxiliary arithmetic device terminated the task which has just been under execution.

Thereby, it is possible to receive the task processing demand outputted from the main arithmetic device by the auxiliary arithmetic

device, without putting the main arithmetic device in a waiting state, and to make the demanded task after terminating the processing of the task which B under execution performed by the auxiliary arithmetic device.

According to claim 2 of the present invention, in the digital signal processor as defined in claim 1, wherein the auxiliary arithmetic device has a priority judgment circuit for determining the priority for performing the processing of the task, for which the processing is demanded, to execute the processing, and the auxiliary arithmetic device performs the task in accordance with the priorities of respective tasks determined by the priority judgment circuit.

Thereby, it is possible to perform the task demanded from the main arithmetic device to the auxiliary arithmetic device in accordance with the determined priorities.

According to claim 3 the present invention, in the digital signal processor as defined in claim 1, wherein the auxiliary arithmetic device has an interruption signal generation circuit for generating an interruption signal interrupting the processing which is under execution, and when receiving the task demand from the main arithmetic device, the auxiliary arithmetic device interrupts the processing and performs the task demanded from the main arithmetic device.

Thereby, it is possible to perform the task, for the processing is demanded from the main arithmetic device with no waiting time by

the auxiliary arithmetic device.

BRIEF DIESCRIPTION OF DRAWINGS

Figure 1 is a block diagram illustrating the construction of a digital signal processor provided with a reservation processing register according to a first embodiment of the present invention.

Figure 2 is a timing chart of the digital signal processor which is provided with the reserv processing register according to the first embodiment.

Figure 3 is a block diagram illustrating the construction of a digital signal processor which is provided with a priority judgment circuit according to a second embodiment of the present invention.

Figure 4 is a timing chart of the digital signal processor provided with the priority judgment circuit according to the second embodiment.

Figure 5 is a block diagram illustrating the construction of a digital signal processor provided with a processing interruption circuit according to a third embodiment of the present invention.

Figure 6 is a timing chart of the digital signal processor provided with the processing interruption circuit according to the third embodiment.

Figure 7 is a block diagram showing the construction of a conventional digital signal processor.

Figure 8 is a timing chart of the conventional digital signal processor.

Figure 9 is a constitutional diagram of a typical optical disk apparatus.

BEST MODE TO EXECUTE THE INVENTION

Hereinafter, embodiments of the present invention will be described with reference to the drawings.

(Embodiment 1)

Figure 1 is a block diagram illustrating the construction of a digital signal processor according to a first embodiment. In figure 1, reference numerals 11 and 12 denote arithmetic devices, numeral 13 denotes an external bus, numerals 14 and 16 denote program memory areas, numerals 15 and 17 denote arithmetic logic units, numeral 18 denotes a task list, numeral 19 denotes an external start-up factor, numeral 20 denotes a processing pointer, numeral 21 denotes a program counter, numeral 22 denotes an instruction decoder, numeral 23 denotes a program halt notification signal, numeral 24 denotes a termination status storage register, numeral 25 denotes a processing demand generation circuit, numeral 26 denotes a reserved processing register, and numeral 27 denotes a clear circuit.

Similarly as the conventional construction shown in figure 7, the arithmetic device 11 and the arithmetic device 12 are connected to each other by the external bus 13, and the arithmetic device 11 can refer to the internal register of the arithmetic device 12. The arithmetic device 11 makes the arithmetic logic unit 15 operate in accordance with a program stored in the program memory area 14, to

calculate driving values required for the spindle control, the traverse control, or the like. Similarly, the arithmetic device 12 also makes the arithmetic logic unit 17 operate in accordance with a program stored in the program memory area 16, to calculate driving values required for the focus control, the tracking control, or the like.

For example, a processing A which is a focus control processing and a processing B which is a tracking control processing in the arithmetic device 12 are previously transferred from the arithmetic device 11 via the external bus 13 and are stored in the program memory area 16. Moreover, starting addresses of the processing A and the processing B are transferred from the arithmetic device 11 to the task list 18 established in the arithmetic device 12. The task list 18 stores the starting addresses of respective processings and execution modes of respective processings as a pair, respectively. The execution mode indicates whether the corresponding processing can be performed or not. When a "Hi" pulse is inputted to the external start-up factor 19 which is generated at a constant period, the arithmetic device 12 initializes the processing pointer 20 so that it indicate the head of the task list 18. Further, "0" indicating no conclusion is set to the termination status storage device 24. In addition, the arithmetic device 12 copies the address stored in the task list 18 that is indicated by the processing pointer 20 to the program counter 21. At this time, when the execution mode corresponding to the address indicated by the processing pointer 20

indicates "0" meaning incapability of execution, the processing pointer 20 is incremented by "1" and attempts to copy the address of the following processing to the program counter 21.

By the above-described operation, the program of the processing A is activated and is read out from the program memory area 16. Then, when the program of the processing A read out is interpreted by the instruction decoder 22, the arithmetic logic unit 17 is operated to perform the processing A. When the program counter 21 reaches the termination address of the processing A and the program halt instruction is inputted to the instruction decoder 22, the arithmetic device 12 makes the instruction decoder 22 output the program halt notification signal 23 to the processing pointer 20. When the program halt notification signal 23 is notified to the processing pointer 20, the arithmetic device 12 changes the indication destination to the task list 18 from the processing A to the processing B and copies the starting address of the processing B to the program counter 21. Thereby, the program of the processing B is activated to perform the processing B.

The arithmetic device 12 repeats similar operations for all processings stored in the task list 18. When all the processings are terminated, while in the conventional method shown in figure 7, 1 indicating the conclusion of the processing was set to the termination status storage register 24, the digital signal processor according to the present invention examines the execution mode in the reservation processing register 26. If assumed that during when

the arithmetic device 12 is performing the processing A or the processing B the address of the processing C is written into the address part of the reservation processing register 26 in the arithmetic device 12 from the arithmetic device 11 and further, "1" indicating capability of execution is written into the execution mode in the reservation processing register 26 during when the arithmetic device 12 is performing the processing A or the processing B, the arithmetic device 12 terminates all the processings stored in the task list 18 and examines the execution mode in the reservation processing register 26. Then, the arithmetic device 12 recognizes that "1" is stored in the execution mode in the reservation processing register 26 and copies the address in the reservation processing register 26 to the program counter 21. Thereby, the program of the processing C is activated and it is read out from the program memory area 16. Then, when the program of the processing C read out is interpreted by the instruction decoder 22, the arithmetic logic unit 17 is operated to perform the processing C. The clear circuit 27 detects that the address in the reservation processing register 26 is copied to the program counter 21, and sets "0" meaning incapability of execution to the execution mode in the reserved processing register 26. When the program counter 21 reaches the termination address of the processing C and the program halt instruction is inputted to the instruction decoder 22, the arithmetic device 12 makes the instruction decoder 22 output the program halt notification signal 23 to the processing pointer 20, and sets "1" indicating the

termination of the processing to the termination status storage register 24.

According to the so-constructed digital signal processor of this first embodiment, the arithmetic device 12 is able to receive the task processing demand outputted from the arithmetic device 11 without making the arithmetic device 11 in a waiting state, and to perform the demanded task after the arithmetic device 12 terminates the task which is under execution. For example, as shown in the timing chart in figure 2, when the processing C execution demand is generated at the arithmetic device 11 while the arithmetic device 12 is performing the processing A, in the conventional digital signal processor, the arithmetic device 11 had to wait with monitoring the termination status storage register 24 until the arithmetic device 12 terminates the processing A and the processing B. However, according to the digital signal processor of the present invention, the arithmetic device 11 can perform the processing C only by writing the address of the processing C into the address part of the reservation processing register 26 as well as writing "1" indicating capability of execution into the execution mode in the reservation processing register 26.

Further, since the digital signal processor of this first embodiment includes additionally the clear circuit 27 which detects that the address in the reservation processing register 26 is copied to the program counter 21 and sets "0" meaning incapability of execution to the execution mode in the reservation processing

register 26, it is possible to perform the processing C, for which the processing is demanded from the arithmetic device 11, only once. For example, as shown in the timing chart in figure 2, if the address and the execution mode of the processing C are added to the task list 18 when the processing C execution demand is generated at the arithmetic device 11 while the arithmetic device 12 is performing the processing A, the processing C will be undesirably performed twice during the sample timing 1 of the arithmetic device 11 because the sample timing 2 of the arithmetic device 12 is operating at a period twice as that of the sample timing 1 of the arithmetic device 11. More specifically, it is assumed that the processings for the focus control and the tracking control are performed in the arithmetic device 12 at a period of 360KHz, while the processings for the spindle control, the traverse control, and the like are performed in the arithmetic device 11 at a period of 180KHz. Here, it is supposed that a part of the processing for the spindle control needs to be performed in the arithmetic device 12 once for every two periods of the arithmetic device 11, i.e., at a period of 90KHz. In such case, by employing the reservation processing register 26, the arithmetic device 11 can demand the arithmetic device 12 to perform the processing so that only a part of the processing for the spindle control may be performed once without a waiting time.

(Embodiment 2)

Figure 3 is a block diagram illustrating the construction of a digital signal processor according to a second embodiment. In

figure 3, reference numerals 11 and 12 denote arithmetic devices, numeral 13 denotes an external bus, numerals 14 and 16 denote program memory areas, numerals 15 and 17 denote arithmetic logic units, numeral 18 denotes a task list, numeral 19 denotes an external start-up factor, numeral 21 denotes a program counter, numeral 22 denotes an instruction decoder, numeral 23 denotes a program halt notification signal, numeral 24 denotes a termination status storage register, numeral 25 denotes a processing demand generation circuit, numeral 26 denotes a reservation processing register, and numeral 27 denotes a clear circuit. The structure is almost similar to that in figure 1 of the first embodiment. A difference from the structure in figure 1 of the first embodiment is that a priority judgment circuit 30 is added in place of the processing pointer 20.

When the program counter 21 reaches the termination address of the processing and the program halt instruction is inputted to the instruction decoder 22, the priority judgment circuit 30 receives the program halt notification signal 23 from the instruction decoder 22. At this time, while the processing pointer 20 in the fist embodiment increments the indication destination to the task list 18 by 1 to judge whether the execution mode of a new indication destination indicates capability of execution or not, the priority judgment circuit 30 compares the value of the execution mode of a new indication destination, which is the result of incrementing the indication destination to the task list 18 by 1, with the value of the execution mode in the reservation processing register 26, and

copies the processing which has a larger value to the program counter 21. Here, the meanings of the execution modes in the task list 18 and in the reservation processing register 26 here are extended from the meaning in the first embodiment. That is, in the fist embodiment, the execution mode of "0" means incapability of execution and the execution mode of "1" means capability of execution. However, in the second embodiment, the execution mode of "0" means incapability of execution and the execution modes of "1" and more mean capability of execution, and further, the value itself means the degree of priority. The larger the value is, the higher the degree of priority is, which means the corresponding processing is performed first. For example, provided that the bit of the execution mode is 2 bits, three kinds of the degree of priority, i.e., 1, 2, and 3 can be specified.

According to the so-constructed digital signal processor of this second embodiment, the arithmetic device 12 is able to receive the task processing demand outputted from the arithmetic device 11 without making the arithmetic device 11 in a waiting state, and to perform the demanded task after the arithmetic device 12 terminates the task which is under execution. For example, as shown in the timing chart in figure 4, when the processing C execution demand is generated at the arithmetic device 11 while the arithmetic device 12 is performing the processing A, in the conventional digital signal processor, the arithmetic device 11 had to wait with monitoring the termination status storage register 24 until the arithmetic device 12 terminates the processing A and the processing B. However,

according to the digital signal processor of the present invention, the arithmetic device 11 can perform the processing C only by writing the address of the processing C into the address part of the reservation processing register 26 as well as writing "1" indicating capability of execution into the execution mode in the reservation processing register 26.

Further, according to the digital signal processor of the second embodiment, by writing the address of a processing having a higher degree of priority than that of the processing which is scheduled to be performed after the termination of the processing which is under execution into the reservation processing register 26 of the arithmetic device 12 from the arithmetic device 11, the execution of the reserved processing can be made faster.

(Embodiment 3)

Figure 5 is a block diagram illustrating the construction of a digital signal processor according to a third embodiment. In figure 5, reference numerals 11 and 12 denote arithmetic devices, numeral 13 denotes an external bus, numerals 14 and 16 denote program memory areas, numerals 15 and 17 denote arithmetic logic units, numeral 18 denotes a task list, numeral 19 denotes an external start-up factor, numeral 21 denotes a program counter, numeral 22 denotes an instruction decoder, numeral 23 denotes a program halt notification signal, numeral 24 denotes a termination status storage register, numeral 25 denotes a processing demand generation circuit, numeral 26 denotes a reservation processing register, numeral 27 denotes a

clear circuit, numeral 50 denotes a processing pointer B, and numeral 51 denotes an interrupt signal generation circuit. The structure is almost similar to that in figure 1 of the first embodiment. Differences from the structure in figure 1 of the first embodiment is that the processing pointer B 50 is prioded in place of the processing pointer 20 and that the interruption signal generation circuit 51 is newly added.

The interrupt signal generation circuit 51 monitors whether writing into the reservation processing register 26 is performed from the arithmetic device 11 via the external bus 13 or not, and when detecting writing into the reserved processing register 26 is detected it notifies the interrupt signal to the processing pointer B 50.

In a case where the interruption signal is notified from the interruption signal generation circuit 51, when the program counter 21 reaches the termination address of the processing and the program halt instruction is inputted to the instruction decoder 22, the processing pointer B 50 receives the program halt notification signal 23 from the instruction decoder 22. Then, the processing pointer B 50 increments the indication destination to the task list 18 by 1, and judges whether the execution mode of a new indication destination is capable of being executed or not, and when it is judged capable of being executed, it copies the address of the task list 18 to the program counter 21.

Meanwhile, when the interruption signal is notified from the

interrupt signal generation circuit 51, the processing pointer B 50 copies the address in the reservation processing register 26 to the program counter 21. Then, since change the indication destination to the task list 18 is not changed, the arithmetic device 12 performs the processing demanded from the arithmetic device 11, and when the program halt notification signal 23 is notified from the instruction decoder 22, the processing pointer B 50 increments the indication destination to the task list 18 by 1, and judges whether the execution mode of the new indication destination is capable of being executed or not, and when it is judged capable of being executed, it copies the address in the task list 18 to the program counter 21.

According to the so-constructed digital signal processor of this third embodiment, when the arithmetic device 12 receives the task processing demand outputted from the arithmetic device 11 it interrupts the processing of the task which is under execution, and performs processing of the demanded task. For example, as shown in the timing chart in figure 6, when the processing C execution demand is generated at the arithmetic device 11 while the arithmetic device 12 is performing the processing A, in the conventional digital signal processor, the arithmetic device 11 had to wait with monitoring the termination status storage register 24 until the arithmetic device 12 terminates the processing A and the processing B. However, according to the digital signal processor of the present invention, the arithmetic device 11 can perform the processing C only by writing the address of the processing C into the address part of the

reservation processing register 26 as well as writing "1" indicating capability of execution into the execution mode of the reserved processing register 26.

Further, according to the digital signal processor of the third embodiment, the processing A which is under execution in the arithmetic device 12 is interrupted by the arithmetic device 11, thereby it is possible to perform the processing C demanded from the arithmetic device 11. At this time, since the processing pointer B 50 does not change the indication destination to the task list 18, the arithmetic device 12 performs the processing B after the execution of the processing C.

APPLICABILITY IN INDUSTRY

As described above, according to the digital signal processor the present invention, the digital signal processor is outputted the task processing demand from the main arithmetic device to the auxiliary arithmetic device and is received in the auxiliary arithmetic device without making the main arithmetic device in a waiting state, thereby it is possible to perform the demanded task after the task that is under execution in the auxiliary arithmetic device is terminated and, more particularly, the digital signal processor is suitable for the arithmetic processing for the servo control in the optical disk apparatus.

CLAIMS

1. A digital signal processor, comprising:

a main arithmetic device which generates a task demand, an auxiliary arithmetic device which receives the task demand from the main arithmetic device and performs the task;

the auxiliary arithmetic device being provided with a reservation processing register for setting a task from the main arithmetic device even when the auxiliary arithmetic device is performing a processing;

a clear circuit for clearing the task stored in the reservation processing register after the task set in the reservation processing register is performed; and

the task demanded from the main arithmetic device being performed after the auxiliary arithmetic device terminated the task which has just been under execution.

2. The digital signal processor as defined in claim 1, wherein

the auxiliary arithmetic device has a priority judgment circuit for determining the priority for performing the processing of the task, for which the processing is demanded, to execute the processing, and

the auxiliary arithmetic device performs the task in accordance with the priorities of respective tasks determined by the priority judgment circuit.

3. The digital signal processor as defined in claim 1, wherein

the auxiliary arithmetic device has an interruption signal generation circuit for generating an interruption signal interrupting the processing which is under execution, and

when receiving the task demand from the main arithmetic device, the auxiliary arithmetic device interrupts the processing and performs the task demanded from the main arithmetic device.

ABSTRACT

A digital signal processor comprises an arithmetic device 12 wherein a reservation processing register 26, to which setting to which from the arithmetic device 11 is possible and which has a construction for storing an address and an execution mode as a task list 18, and a clear circuit 27 for clearing the execution mode when the address in the reservation processing register 26 is copied to a program counter 21, are newly added.

Thereby, in the digital signal processor comprising two arithmetic devices, it is possible to remove the processing waiting time as well as to change the processing order at respective arithmetic devices.

Fig.1

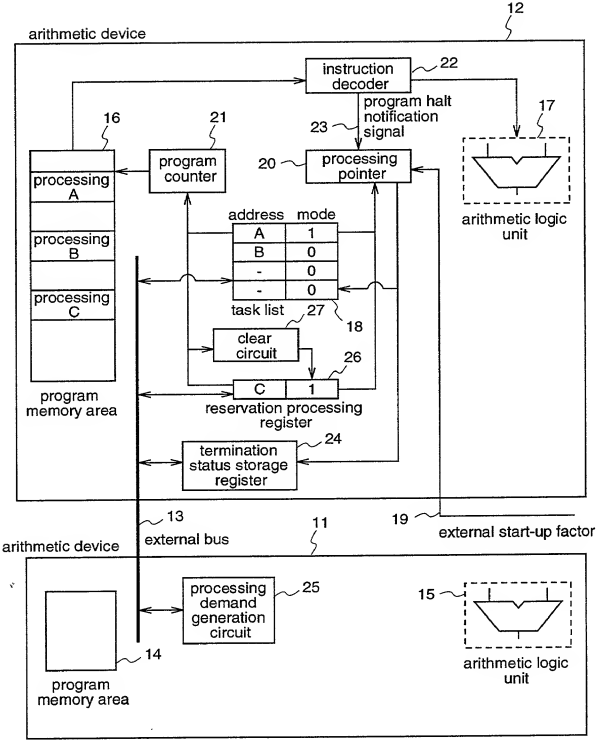

12
arithmetic device
instruction decoder
22
program halt notification signal
23
17
16
21
program counter
20
processing pointer
processing A
processing B
processing C
arithmetic logic unit
address mode
A 1
B 0
- 0
- 0
task list
27
18
clear circuit
26
C 1
program memory area
reservation processing register
24
termination status storage register
13
external bus
11
19
external start-up factor
arithmetic device
processing demand generation circuit
25
15
14
program memory area
arithmetic logic unit

Fig.2

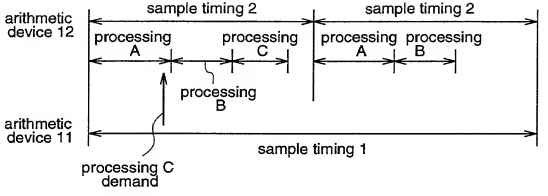

arithmetic device 12
sample timing 2
sample timing 2
processing A
processing C
processing A
processing B
processing B
arithmetic device 11
sample timing 1
processing C demand

Fig.3

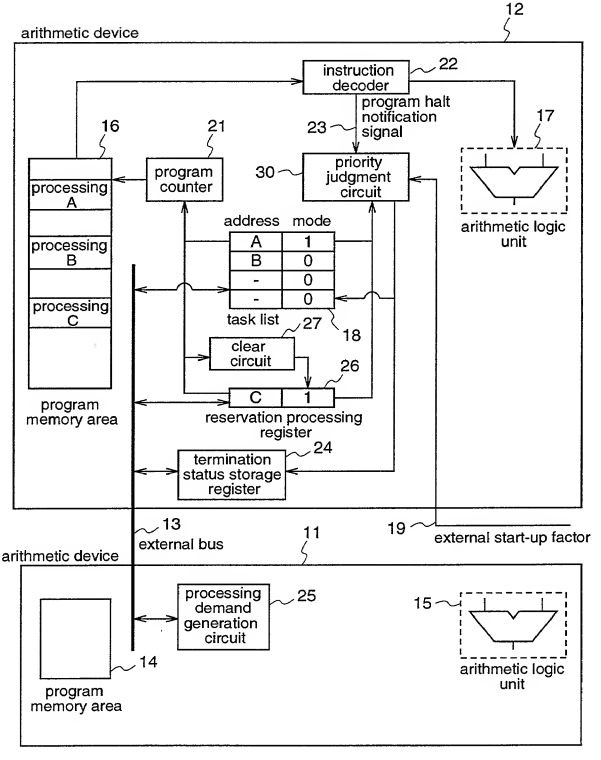

12
arithmetic device
instruction decoder
22
program halt notification signal
23
17
16
21
30
priority judgment circuit
program counter
processing A
processing B
processing C
arithmetic logic unit
address
mode
A
1
B
0
-
0
-
0
task list
27
18
clear circuit
26
C
1
program memory area
reservation processing register
24
termination status storage register
13
external bus
11
19
external start-up factor
arithmetic device
processing demand generation circuit
25
15
14
program memory area
arithmetic logic unit

Fig.4

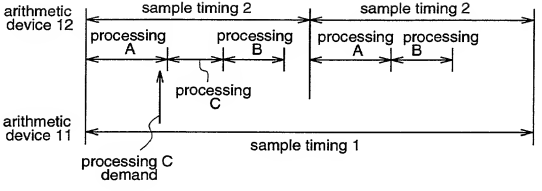


Fig.5

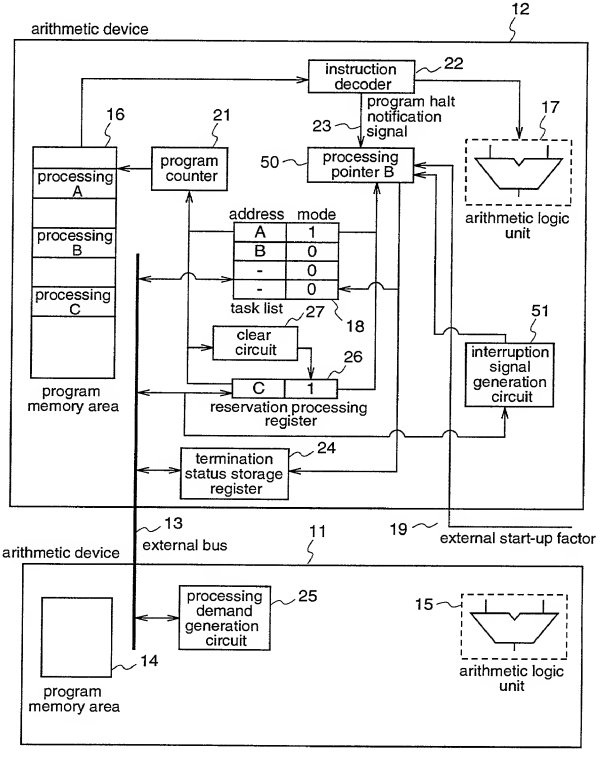

12
arithmetic device
instruction decoder
22
program halt notification signal
23
17
16
21
program counter
50
processing pointer B
processing A
processing B
processing C
arithmetic logic unit
address mode
A 1
B 0
- 0
- 0
task list
27
18
clear circuit
51
26
interruption signal generation circuit
C 1
program memory area
reservation processing register
termination status storage register
24
13
external bus
11
19
external start-up factor
arithmetic device
processing demand generation circuit
25
15
14
program memory area
arithmetic logic unit

Fig.6

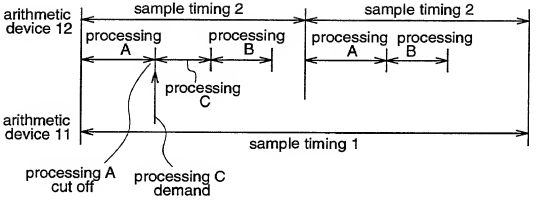


Fig.7

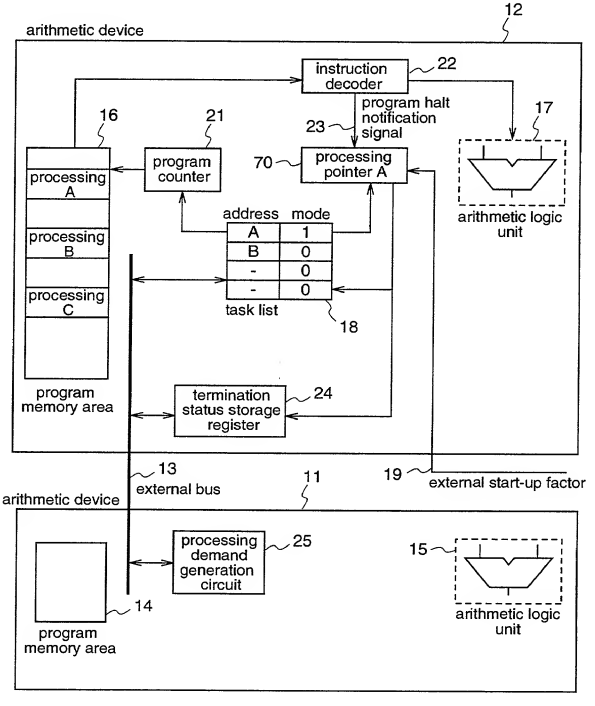

12
arithmetic device
instruction decoder
22
program halt notification signal
23
17
16
21
processing A
program counter
70
processing pointer A
processing B
processing C
address mode
A 1
B 0
- 0
- 0
task list
18
arithmetic logic unit
program memory area
termination status storage register
24
13
external bus
11
19
external start-up factor
arithmetic device
processing demand generation circuit
25
15
14
program memory area
arithmetic logic unit

Fig.8

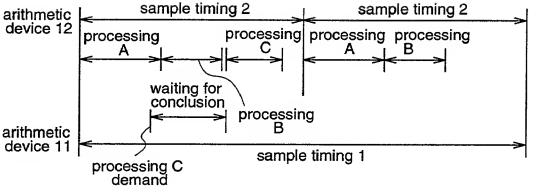
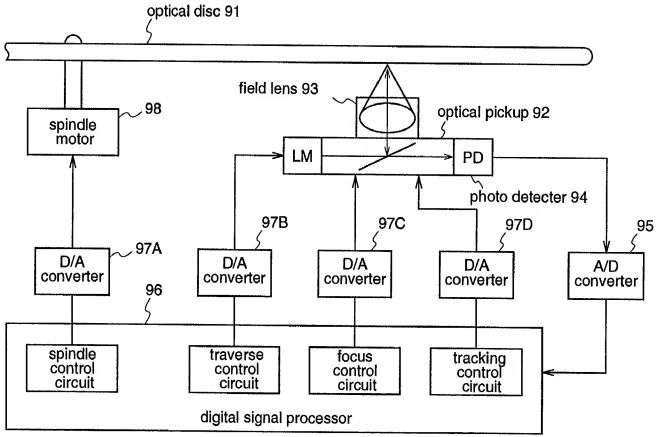


Fig.9



Rev. 1-16-01 Effective March 1998

DECLARATION AND POWER OF ATTORNEY FOR U.S. PATENT APPLICATION

() Original () Supplemental () Substitute (X) PCT () DESIGN

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Title: DIGITAL SIGNAL PROCESSOR

of which is described and claimed in:
() the attached specification, or
() the specification in application Serial No. NEW, filed March 6, 2001, and with amendments through _____, or
(X) the specification in International Application No. PCT/JP00/04475, filed July 5, 2000, and as amended on (if applicable).

I hereby state that I have reviewed and understand the content of the above-identified specification, including the claims, as amended by any amendment(s) referred to above.

I acknowledge my duty to disclose to the Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I hereby claim priority benefits under Title 35, United States Code, §119 (and §172 if this application is for a Design) of any application(s) for patent or inventor's certificate listed below and have also identified below any application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

COUNTRY	APPLICATION NO.	DATE OF FILING	PRIORITY CLAIMED
Japan	No.Hei.11-191143	July 6, 1999	YES

I hereby claim the benefit under Title 35, United States Code §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose information material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION SERIAL NO.	U.S. FILING DATE	STATUS: PATENTED, PENDING, ABANDONED

And I hereby appoint Michael R. Davis, Reg. No. 25,134; Matthew M. Jacob, Reg. No. 25,154; Warren M. Cheek, Jr., Reg. No. 33,367; Nils Pedersen, Reg. No. 33,145; Charles R. Watts, Reg. No. 33,142; and Michael S. Huppert, Reg. No. 40,268, who together constitute the firm of WENDEROTH, LIND & PONACK, L.L.P., as well as any other attorneys and agents associated with Customer No. 000513, to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected therewith.

I hereby authorize the U.S. attorneys and agents named herein to accept and follow instructions from HAYASE & CO. as to any action to be taken in the U.S. Patent and Trademark Office regarding this application without direct communication between the U.S. attorneys and myself. In the event of a change in the persons from whom instructions may be taken, the U.S. attorneys named herein will be so notified by me.

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Post Office Address	ADDRESS	CITY	STATE OR COUNTRY	ZIP CODE
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Residence & Citizenship	CITY	STATE OR COUNTRY	COUNTRY OF CITIZENSHIP	
Post Office Address	ADDRESS	CITY	STATE OR COUNTRY	ZIP CODE

I further declare that all statements made herein of my own knowledge are true, and that all statements on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

1st Inventor Yasushi Imamura Date 2001.4.10
Yasushi IMAMURA

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Takao INOUE

3rd Inventor Masaaki Okita Date 2001.4.10
Masaaki OKITA

4th Inventor _____ Date _____

5th Inventor _____ Date _____

6th Inventor _____ Date _____

The above application may be more particularly identified as follows:

U.S. Application Serial No. NEW Filing Date March 6, 2001

Applicant Reference Number P-23074-02 Atty Docket No. 2001-0244A

Title of Invention DIGITAL SIGNAL PROCESSOR